REMARKS

Entry of the above amendments to the claims is requested prior to examination on the merits.

By the foregoing amendment, claims 1, 4, 7, 11, 12 and 15-20 have been amended and new claims 21-26 have been added. No new matter is added by the foregoing amendment, and the amendment is fully supported by the specification. Thus, claims 1-26 are currently pending in the application and subject to examination.

In the Office Action mailed January 24, 2006, the Examiner rejected claims 1-20 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Independent claims 1, 7, 11 and 15 have been amended responsive to this rejection. If any additional amendment is necessary to overcome this rejection, the Examiner is requested to contact the Applicant's undersigned representative.

In the outstanding Office Action, the Examiner rejected claims 1-3, 5-11 and 13-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,784,933 to Nakai (hereinafter, "Nakai"). Under 35 U.S.C. § 103(a), the Examiner rejected claims 4, 12 and 19 under 35 U.S.C. § 103(a), as being unpatentable over Nakai in view of U.S. Patent No. 6,060,742 to Chi et al. (hereinafter, "Chi et al."), and claim 20 under 35 U.S.C. § 103(a), as being unpatentable over Nakai in view of U.S. Patent No. 6,501,109 to Chi (hereinafter, "Chi"). It is noted that claims 1, 4, 7, 11, 12 and 15-20 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicant hereby traverses the rejections, as follows.

In each of independent claims 1, 7, and 11, as amended, a solid state image pickup device includes a first region of a first conductivity type, a first gate structure, and

a second region of the first conductivity type, which together form a non-volatile memory element. In claims 1, 7, and 11, the first region is electrically floating and the second region is connected to a wiring line for applying a voltage thereto. Independent claim 15 recites a method with similar features.

The solid state image pickup device of Nakai is different from that of the claimed invention, at least because both n-type regions 17 of Nakai are electrically floating, requiring two transistors SGS and SGD to allow current to flow between the nonvolatile memory gate. In addition, Nakai discloses only F-N tunneling injection between the p-type well 12 and the floating gate 14 for carrier injection. Since the n-type regions 17 on both sides of the photoelectric converting element PD are floating, a lateral electric field is not created in the photoelectric converting element PD. Thus, electrons due to drift are not accelerated to become "hot" electrons in the device of Nakai. Moreover, Nakai discloses at col. 1, lines 57-63, that writing by hot carrier injection is not practical.

In view of the above, the Applicant submits that none of the applied art of record, nor combination thereof, discloses or suggests at least the combination of a first region of the first conductivity type formed in said second layer and constituting a photodiode with said second layer, the first region being electrically floating and capable of storing charge carriers; a first gate structure including a charge storage region and a control gate, said first gate structure being formed on a surface of said semiconductor substrate adjacent to a portion of said first region, and said charge storage region being isolated from said first region; a second region of the first conductivity type formed in said second layer adjacent to said first gate structure on a side opposite to said first region, and constituting a non-volatile memory element with said first region and said first gate

structure; a first wiring connected to said second region for applying a voltage to said second region; a light shielding film formed above said first gate structure and having an aperture above said first region, and a control circuit for applying a first write voltage to the control gate of said first gate structure, the first write voltage being a write voltage for tunneling and injecting charges accumulated in said first region into the charge storage region, as recited in claim 1, as amended.

For at least this reason, the Applicant submits that claim 1, as amended, is allowable over the applied art of record. As claim 1 is allowable, the Applicant submits that claims 2-6, as well as new claims 21 and 22, each of which depends from allowable claim 1, are likewise allowable over the applied art of record.

Similarly to as discussed above with regard to claim 1, the Applicant submits that claim 7 is allowable over the applied art of record at least because the applied art of record, and any combination thereof, fails to disclose or suggest the combination of a first region of the first conductivity type formed in the second layer and constituting a photodiode with the second layer, the first region being electrically floating; a first gate structure including a charge storage region and a control gate, the first gate structure being formed on a surface of the semiconductor substrate adjacent to a portion of the first region, and the charge storage region being isolated from the first region; a second region of the first conductivity type constituting a non-volatile memory element with the first region and the first gate structure, formed in the second layer adjacent to the first gate structure on a side opposite to the first region; a first wiring connected to the second region for applying a voltage to the second region; a light shielding film formed above the first gate structure and having an aperture above the first region a second

gate structure of an insulated gate type formed on the surface of the semiconductor substrate, adjacent to another portion of the first region; and a third region of the first conductivity type formed in the second layer, adjacent to the second gate structure on a side opposite to the first region, the third region constituting an insulated gate type transistor with the first region and the second gate structure, as recited in claim 7, as amended.

As claim 7 is allowable, the Applicant submits that claims 8-10, as well as new claims 23 and 24, each of which depends from allowable claim 7, are likewise allowable over the applied art of record.

The Applicant further submits that none of the applied art of record, nor combination thereof, discloses or suggests at least the combination of a first region of the first conductivity type formed in said second layer and constituting a photodiode with said second layer, the first region being electrically floating; a first gate structure including a charge storage region and a control gate, said first gate structure being formed on a surface of said semiconductor substrate adjacent to a portion of said first region, and said charge storage region being electrically isolated from said first region; a second region of the first conductivity type formed in the second layer, adjacent to said first gate structure on a side opposite to said first region, and constituting a non-volatile memory element with said first region and said first gate structure; a first wiring connected to said second region for applying a voltage to said second region; a light shielding film formed above said first gate structure and having an aperture above said first region, as recited in claim 11, as amended.

For at least this reason, the Applicant submits that claim 11, as amended, is allowable over the applied art of record. As claim 11 is allowable, the Applicant submits that claims 12-14, as well as new claims 25 and 26, each of which depends from allowable claim 11, are likewise allowable over the applied art of record.

In addition, the Applicant submits that none of the applied art of record, nor combination thereof, discloses or suggests at least the combination of each of said photodiodes including a first region of said first conductivity type formed in said second layer, the first region being electrically floating, said solid state image pickup device having a gate structure including a control gate and a charge storage region, and formed on the second layer adjacent said first region, said charge storage region being electrically isolated from said first region, a drain region of said first conductivity type formed in the second layer adjacent to the gate structure on a side opposite to said first region, a first wiring connected to said drain region, a second wiring connected to said first layer, and a light shielding film formed above said semiconductor substrate and having apertures respectively above the first regions of said photodiodes; (b) applying a first write control voltage to said control gate for tunneling and injecting at least a portion of charges stored in said first region representative of the image information into the charge storage region as signal charges; and (c) applying read control voltages to the drain region through said first wiring and to the control gate to detect a threshold voltage corresponding to an amount of the signal charges injected at said step (b) into the charge storage region, recited in claim 15, as amended.

For at least this reason, the Applicant submits that claim 15, as amended, is allowable over the applied art of record. As claim 15 is allowable, the Applicant submits

that claims 16-20, each of which depends from allowable claim 15, are likewise allowable over the applied art of record.

In addition, with regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

In the Office Action, the Examiner merely states that the motivation for combining the references is found in certain advantages stated by the Examiner (see, e.g., page 7, lines 2-5 and 13-15 of the Office Action). The Examiner, however, indicates nothing from within the applied references to evidence the desirability of this combination. This is an insufficient showing of motivation.

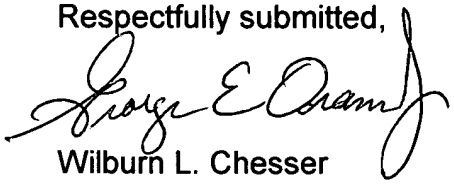
CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing docket number 107317-00061.

Respectfully submitted,



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